ON CHIP TIMING ADJUSTMENT IN MULTI-CHANNEL FAST DATA TRANSFER

Abstract of the Disclosure

A method and structure for an apparatus for maintaining signal integrity between integrated circuits residing on a printed circuit board. The apparatus has adjustable delay circuitry within the circuits and the adjustable delay circuitry adjusts the timing of signals processed within the circuit. A phase monitor connects to the circuits. The phase monitor detects phase differences between signals output by the circuits. A controller connected to the delay circuitry, the phase monitor, and the controller adjust the delay circuitry to compensate for the phase differences.